WHAT IS CLAIMED IS:

1. A reproduction signal processing device, comprising:

an A/D converter for quantizing an input analog reproduction signal into digital reproduction signal data;

an adaptive equalizer for equalizing the reproduction signal data with a characteristic controlled according to data input to the adaptive equalizer and data output from the adaptive equalizer; and

a PLL circuit for outputting a clock signal which is in synchronization with the reproduction signal data;

an analog filter for removing noise from the reproduction signal; and

a digital filter provided between the A/D converter and the adaptive equalizer, the digital filter equalizing the reproduction signal data with a fixed characteristic,

wherein the PLL circuit outputs the clock signal based on an output of the digital filter.

2. A reproduction signal processing device according to claim 1, wherein the analog filter has a low pass characteristic.

3. A reproduction signal processing device according to claim 1, wherein the digital filter has a high band emphasis characteristic.

4. A reproduction signal processing device according to claim 3, wherein the digital filter has a low pass characteristic which allows the passage of a lower frequency component as compared with the analog filter.

5. A reproduction signal processing device according to claim 1, wherein the digital filter is a FIR filter which has a characteristic determined according to one or more tap coefficients set in the digital filter.

6. A reproduction signal processing device according to claim 1, further comprising a control section for determining the fixed characteristic of the digital filter prior to the start of reproduction signal processing.

7. A reproduction signal processing device according to claim 6, wherein:

the digital filter is a FIR filter which has a characteristic determined according to one or more tap coefficients set in the digital filter; and

the control section sets any of a plurality of tap coefficient candidate values in the digital filter, thereby determining the fixed characteristic of the digital filter.

8. A reproduction signal processing device according to claim 6, wherein the control section determines the fixed characteristic of the digital filter based on a value corresponding to a phase error in the PLL circuit.

9. A reproduction signal processing device according to claim 6, wherein the control section determines the fixed characteristic of the digital filter based on an equalization error in the adaptive equalizer.

10. A reproduction signal processing device according to claim 6, wherein the control section determines the fixed characteristic of the digital filter based on a difference between data input to the adaptive equalizer and data output from the adaptive equalizer.

11. A reproduction signal processing device according to claim 6, wherein prior to the start of reproduction signal processing, the control section synthesizes a predetermined characteristic with a characteristic converged by the operation of the adaptive equalizing filter and sets the synthesized characteristic as the fixed characteristic of the digital filter.

12. A reproduction signal processing device according to claim 11, wherein:

each of the digital filter and the adaptive equalizer includes a FIR filter which has a characteristic determined according to one or more tap coefficients; and

the control section sets, as the tap coefficient in the digital filter, a value obtained by the sum-of-products operation of the tap coefficient determined such that the digital filter has the predetermined characteristic and the tap coefficient determined such that the adaptive equalizer has the converged characteristic.

13. A reproduction signal processing device according to claim 1, wherein the PLL circuit outputs a first clock signal for driving the adaptive equalizer and a second clock signal for driving the A/D converter and the digital filter, the second clock signal having a frequency that is N times higher than that of the first clock signal where N is an integer equal to or greater than 2.

14. A reproduction signal processing device according to claim 1, wherein:

the reproduction signal processing device reads recorded data from a recording medium;

the analog filter has a low pass characteristic; and

the upper limit of a frequency component which is allowed to pass through the analog filter is changed according to the speed of reading the recorded data.

15. A reproduction signal processing device according to claim 1, wherein:

the reproduction signal processing device reads recorded data from a recording medium;

the PLL circuit outputs a first clock signal for driving the adaptive equalizer and a second clock signal for driving the A/D converter and the digital filter;

the frequency of the first clock signal is determined according to the speed of reading the recorded data; and

the frequency of the second clock signal is substantially constant irrespective of the speed of reading the recorded data.